BYOC\_HW6 Simulation 3:

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Answer the following questions.

C.1) What are the limitations due to the pipeline latency of the following combinations (assume Data Forwarding already exists):

* beq after add where the add Rd is the beq Rt
* beq after lw where the lw Rt is the beq Rs

Use a similar figure to Fig.2 and Fig. 3 to demonstrate your answers. Explain your answers!

C.1.a - beq after add where the add Rd is the beq Rt

WB

EX

ID

IF

WB

EX

ID

IF

WB

EX

ID

IF

add **$3**,$5,$8

WB

EX

ID

IF

WB

EX

ID

IF

CK

MEM

MEM

MEM

MEM

MEM

EX

C.1.b - beq after lw where the lw Rt is the beq Rs

WB

EX

ID

IF

WB

EX

ID

IF

WB

EX

ID

IF

lw **$3**,16($10)

WB

EX

ID

IF

WB

EX

ID

IF

CK

MEM

MEM

MEM

MEM

MEM

EX

C.2) What are the limitations of all cases of C.1 after you add the Branch Forwarding? . Explain your answers!

C.2.a - beq after add where the add Rd is the beq Rt

WB

EX

ID

IF

WB

EX

ID

IF

WB

EX

ID

IF

add **$3**,$5,$8

WB

EX

ID

IF

WB

EX

ID

IF

CK

MEM

MEM

MEM

MEM

MEM

EX

C.2.b - beq after lw where the lw Rt is the beq Rs

WB

EX

ID

IF

WB

EX

ID

IF

WB

EX

ID

IF

lw **$3**,16($10)

WB

EX

ID

IF

WB

EX

ID

IF

CK

MEM

MEM

MEM

MEM

MEM

EX

C.3) Why can’t we check the result of the previous instruction (time slot n-1) by a beq instruction following it (time slot n)?

מכיוון שבביצוע beq אנחנו מבצעים forwarding ולכן בזמן ביצוע הbranch המידע של ההוראה הקודמת אינו תקף עוד

C.4) List all of the limitations for Assembly programmer you can think of that still exist after adding the Data & Branch Forwarding circuits. . Explain your answer!

ביצוע גישה לזכרון לפני שעברנו את שלב הmem

ביצוע קריאות nop לפעולות ALU בשלבי ex, mem, wb

C5) What is the shortest loop code possible (not an infinite loop)? Any limitations? Explain in detail

Lw $8 0h

Lw $9 (loop length)

Loop operations

Addi $8 $8 4

Bne $8 $9